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thin second spacers disposed adjacent to opposite sides of said thin first spacers wherein said thin second spacers are recessed to lower surface of said conductive layer;

thin third spacers disposed adjacent to opposite sides of said thin second spacers wherein said thin third spacers are recessed to lower surface of said conductive layer; and,

thick fourth spacers disposed adjacent to opposite sides of said thin third spacers wherein said thick fourth spacers are recessed to lower surface of said conductive layer.

32. (Once Amended) The gate electrode of claim 31 wherein said insulative layer comprises an oxide.

33. (Once Amended) The gate electrode of claim 32 wherein said gate layer comprises a polysilicon.

34. (Once Amended) The gate electrode of claim 33 wherein said conductive layer comprises a polycide.

35. (Once Amended) The gate electrode of claim 34 wherein said thin first spacers comprise an oxide.

36. (Once Amended) The gate electrode of claim 35 wherein said thin second spacers comprise a nitride.

*claim*  
37. (Once Amended) The gate electrode of claim 36 wherein said thin third spacers comprise an oxide.

38. (Once Amended) The gate electrode of claim 37 wherein said thick fourth spacers comprise a nitride.

39. (Once Amended) The gate electrode of claim 38 wherein said polycide comprises titanium silicide (TiSi<sub>2</sub>).

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